

Fig. 1

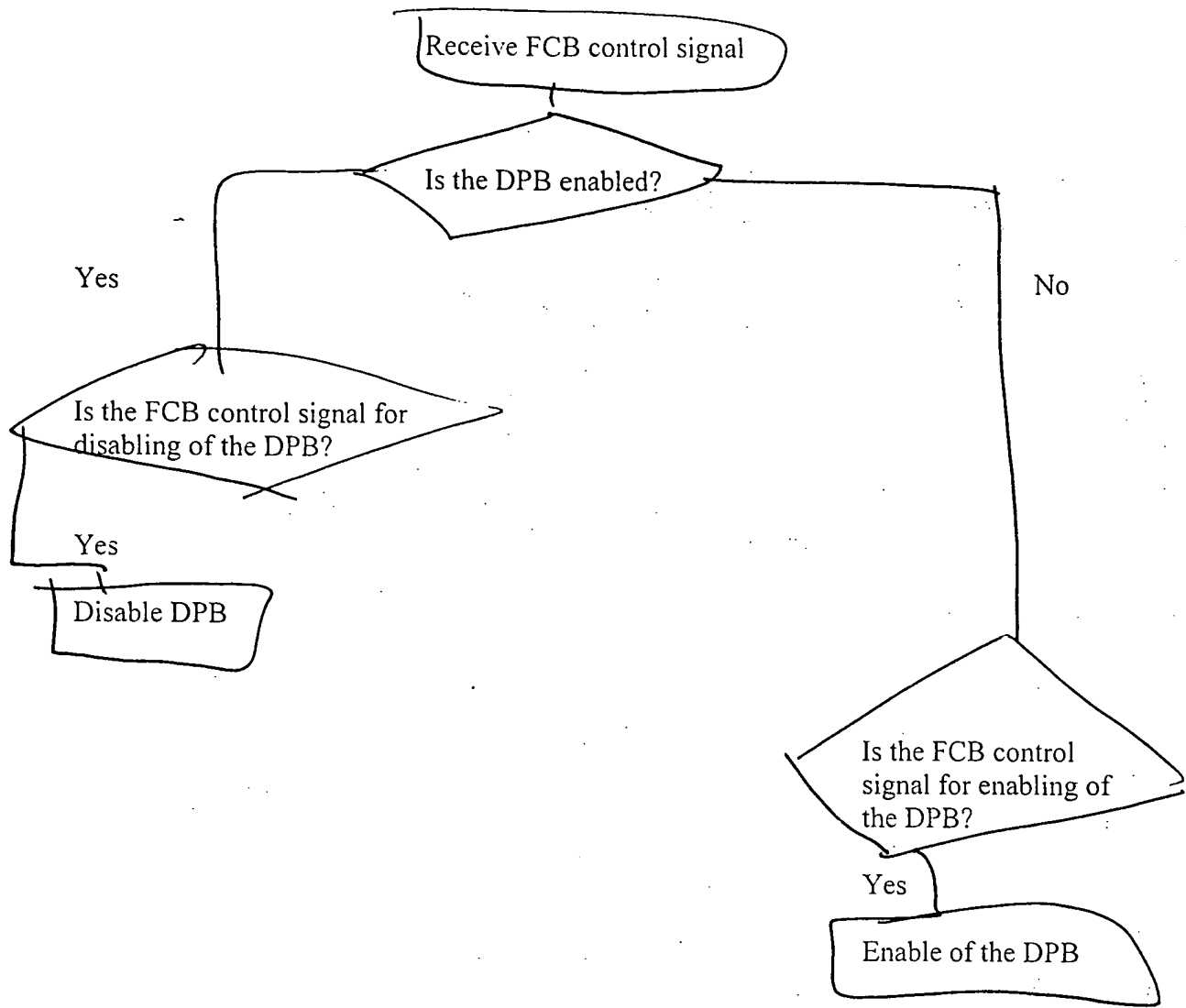


FIG. 2a

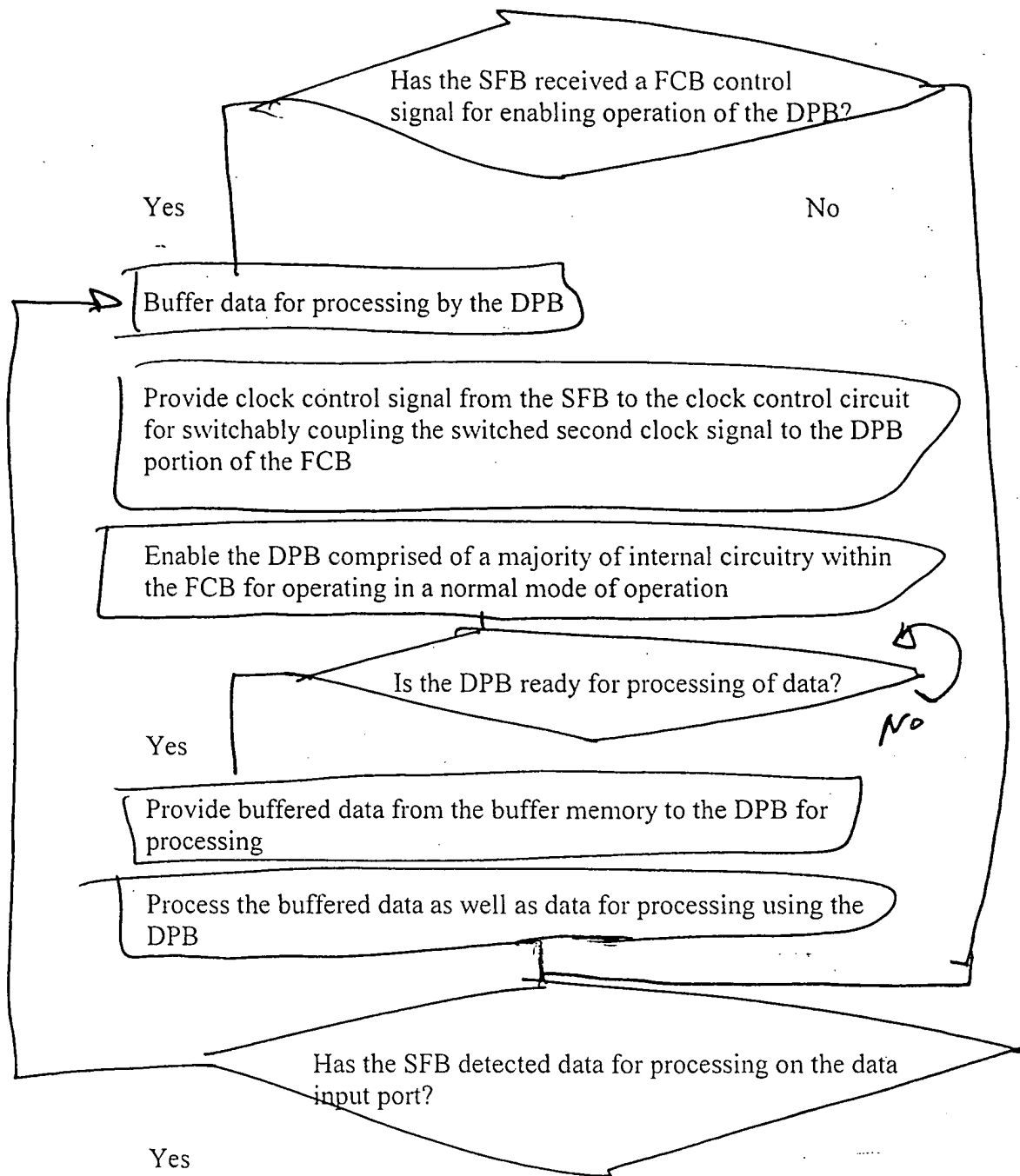


FIG. 2b

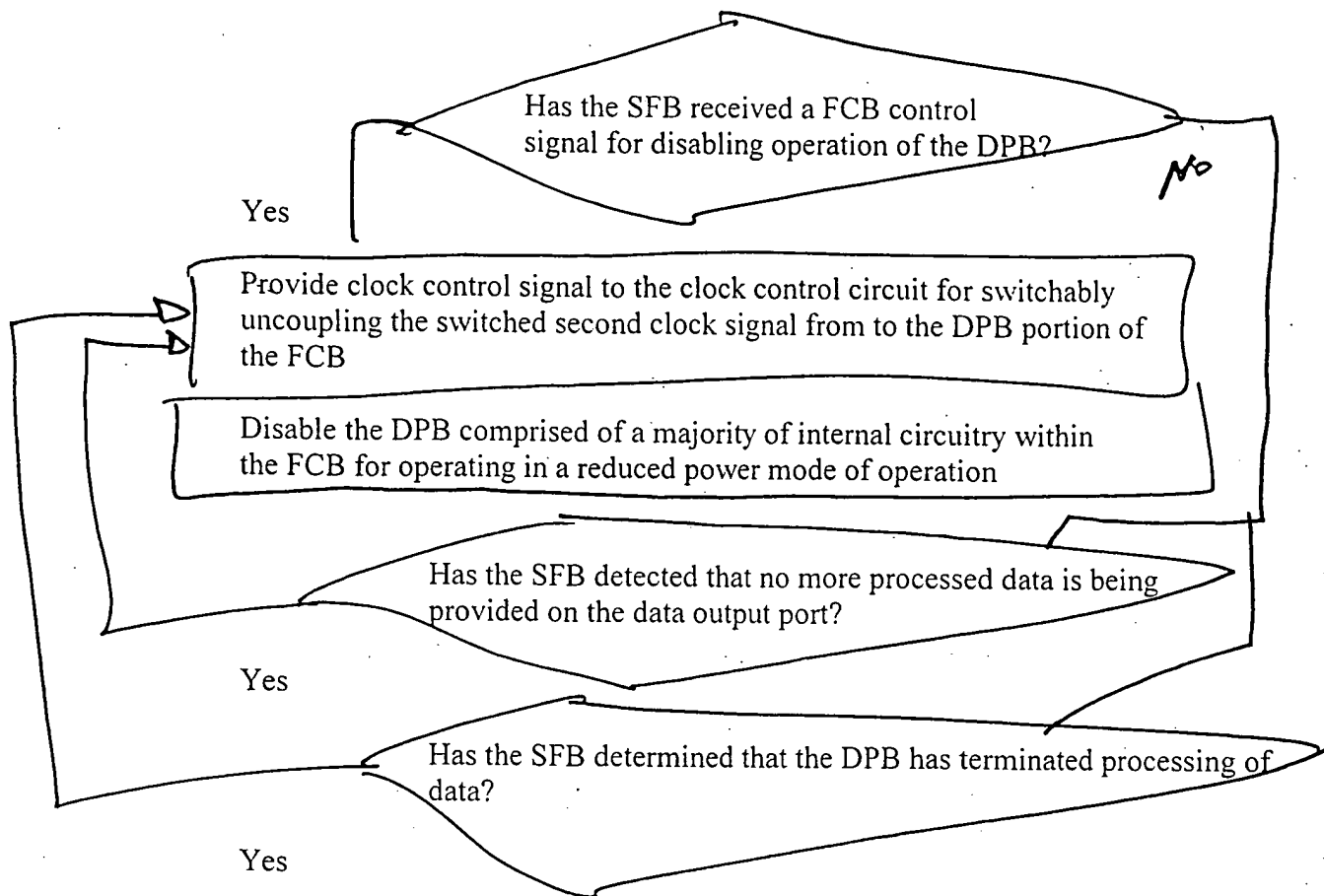


FIG. 2c

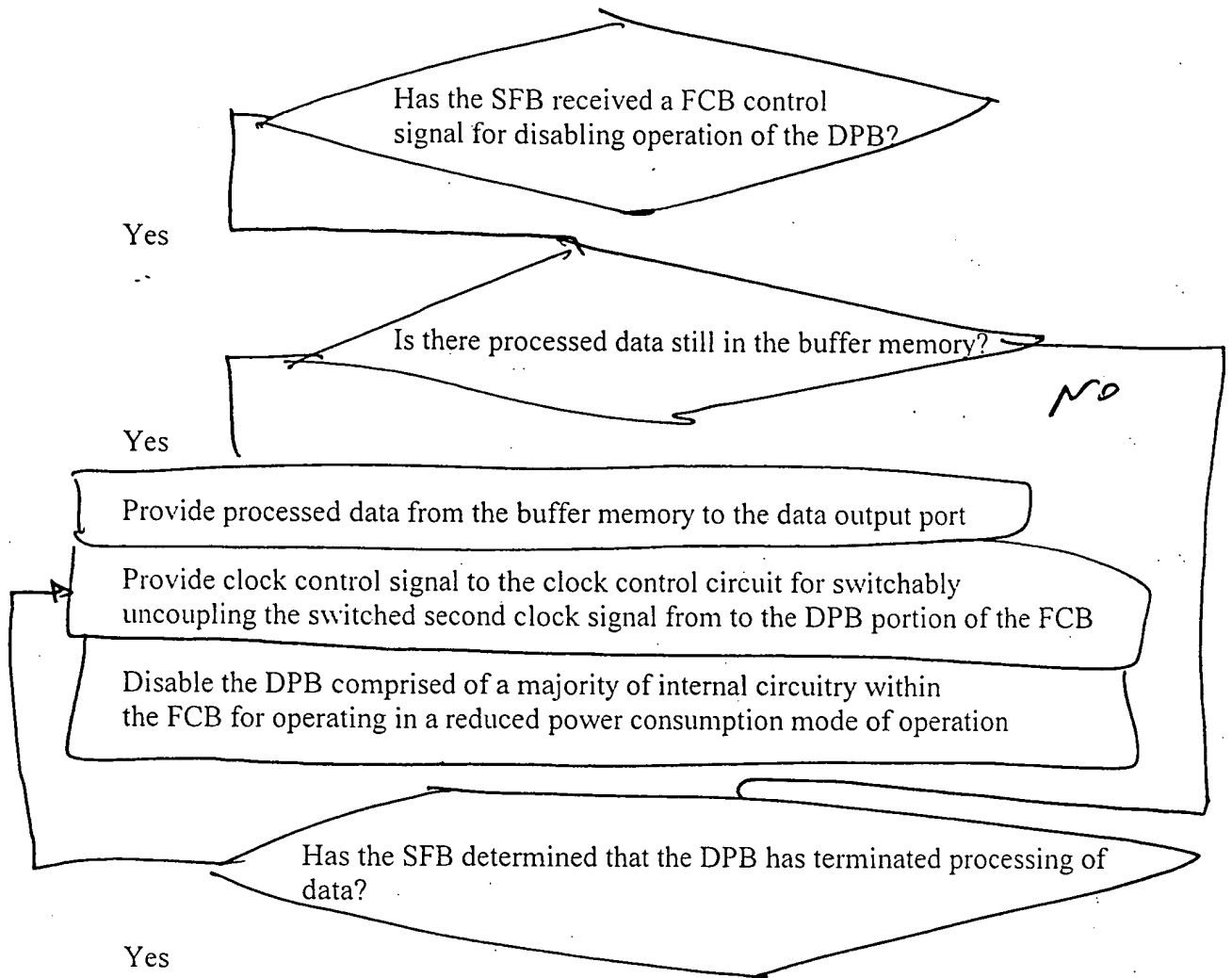


Fig. 2d

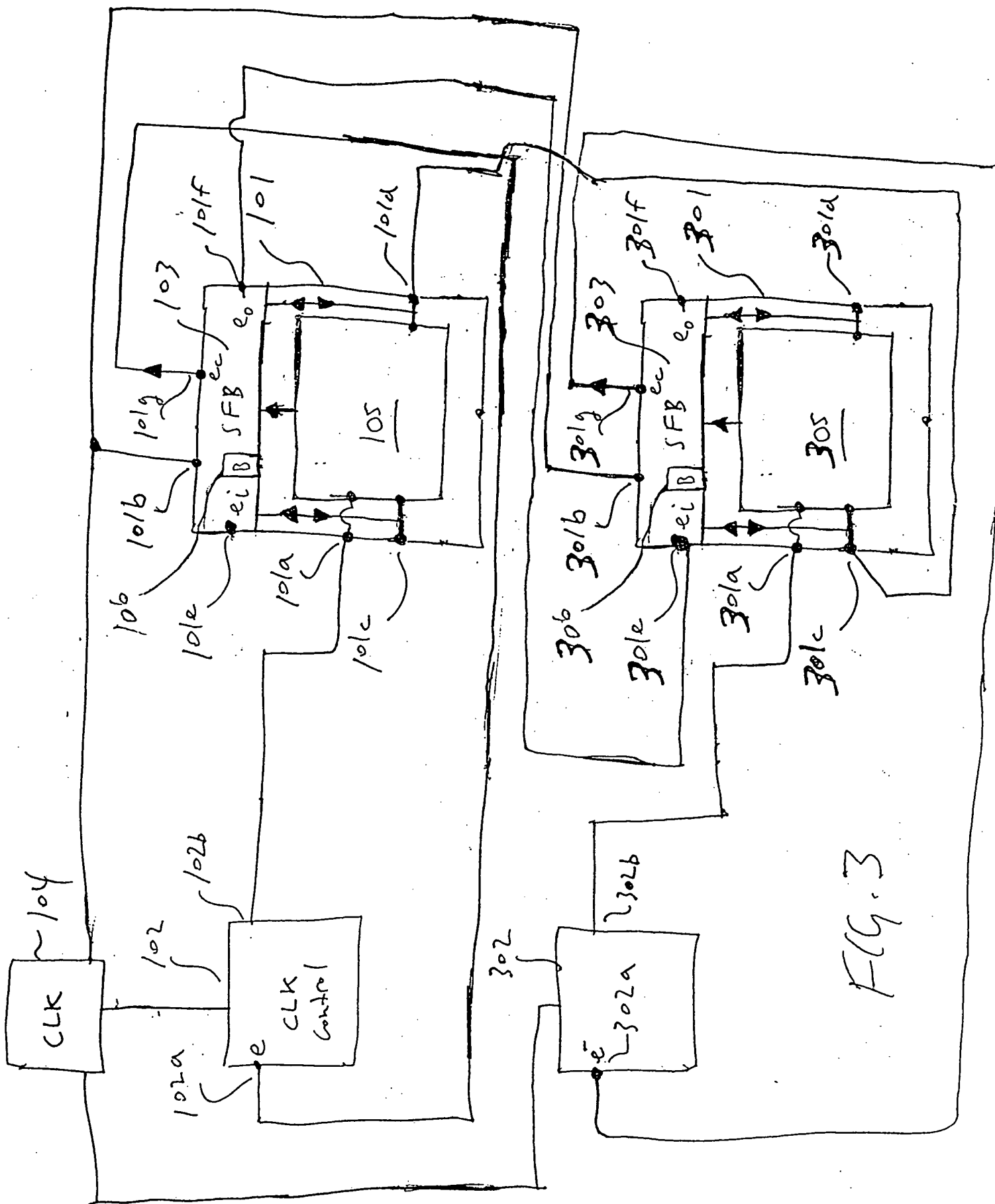


Fig. 3

Buffer data for processing provided on the data input port of the first FCB

Enable of the DPB portion of the first FCB using the SFB disposed in the first FCB

Provide a clock control signal from the first FCB to a first clock control circuit for switchably coupling of the second clock signal to the first FCB

Process data using the first FCB

Buffer processed data within the first FCB prior to providing this data to the second FCB

Provide a FCB control signal from the first FCB to the second FCB for enabling of the second FCB from the plurality of sequentially disposed FCBs

Terminate processing of data in the first FCB

Provide buffered data to the second FCB

Provide a clock control signal from the first FCB to the first clock control circuit for switchably uncoupling of the second clock signal to the first FCB

Disable the DPB portion of the first FCB using the SFB disposed in the first FCB so the first FCB operates in a reduced power consumption mode of operation

Process data using the second FCB.

Buffer processed data within the second FCB prior to providing this data to another FCB

Use the SFB disposed in the second FCB to determine when the second FCB has terminated processing of data

Provide a FCB control signal from the second FCB to another FCB for enabling of the another FCB from the plurality of sequentially disposed FCBs

Terminate processing of data in the second FCB

Provide buffered data to the another FCB

Provide a clock control signal from the second FCB to the second clock control circuit for switchably uncoupling of the third clock signal from the second FCB

Disable the DPB portion of the second FCB using the SFB disposed in the second FCB so the second FCB operates in a reduced power consumption mode of operation.

FIG. 4

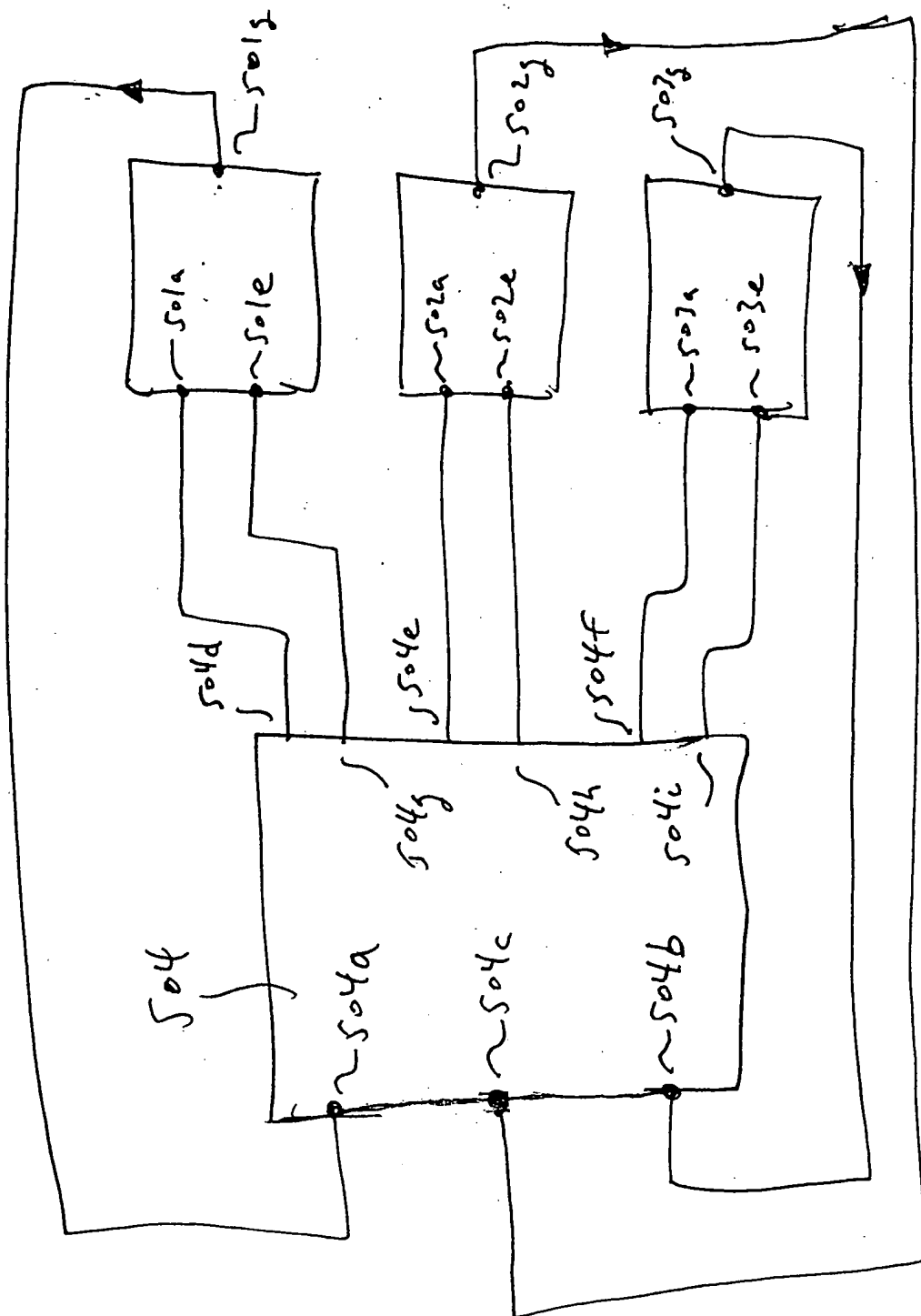


Fig. 5



